REMARKS

Claims 1, 3-14 and 16-26 are currently active.

Antecedent support for the amendments to Claims 1 and 14 is found on page 10, line 24; page 11, line 5 and page 19, line 6.

The Examiner has rejected Claims 1, 3, 4, 14, 16 and 17 as being unpatentable over Sindhu in view of Cyr. Applicants respectfully traverse this rejection.

Referring to Sindhu, there is disclosed a high-speed switching device. Sindhu teaches in a packet switching system, a source 10 is connected to one or more routers 20 for transmitting packets to one or more destinations 30. Each router 20 includes an input switch 100, and output switch 102, a memory 104 including one or more memory banks 105, a controller 106 and a plurality of input and output ports 107 and 108, respectively. Associated with the controller 106 is controller memory 109 for storing a routing table. Packets are received at input port 107, transferred to input switch 100 and stored temporarily in memory 104. When the packet is received by switch 100, a key is read from the first data block in the packet and transferred to controller 106. The key contains destination information which is derived from the header fields associated with the first block of data in a packet. A route

lookup engine 110 and controller 106 performs a search based on the key information and returns a result which includes the output port associated with the destination. Output switch 102 transfers the notification to the identified output port 108. Upon receiving notification information, the output port 108 initiates the transfer of the packet from memory 104 through output switch 102 back to the appropriate input port 108. Each input port 107 includes a line input interface 300, a data handler 304 and a cell output port 306. Packets are received at line input interface 300. As the packets are received, data handler 302 divides the packets received into fixed length cells. As the data handler divides the incoming packet into fixed link cells, it synchronously outputs the cells to input switch 100 through cell output port 306. See column 4, lines 14-61.

Sindhu teaches a single cell is transferred from input port 107 to input switch 100 at each cell slot. The data format for each cell transferred from an input port to input switch 100 includes an internal header and a cell data field. The input switch 100 includes a round robin data handler 500, one or more input port interfaces, one or more memory interfaces, a like plurality of pointers, and output processor 505, one or more port interfaces, and a reservation table 508, an indirect cell processor, controller interface and read controller 516. Round robin data handler 500 receives cells for each input port and transfers them to output processor 505 for output to an appropriate memory bank 105 in memory 104. See column 5, lines 19-41.

Round robin data handler 500 and output processor 505 transfers cells out to memory 104 on transmission lines 460. Round robin data handler 500 time division multiplexes the transfers to output processor 505 such that consecutive cells from the same input port are written to consecutive memory banks 105 in memory 104. Round robin data handler 500 includes a key reading engine 514 for determining the key information associated with a first cell in a packet and a linking engine 515 for linking cells in the same packet. Linking engine 515 determines the starting address in memory for the first cell to a given packet. See column 6, lines 1-34.

As is apparent from the above description, there is no teaching or suggestion of the limitation of sending portions of the packet as stripes to each fabric, let alone there being a plurality of fabrics or a parity fabric which receives a parity strip, as found at applicants' claimed invention.

Referring to Cyr, there is disclosed an asynchronous transfer mode switch architecture. Cyr teaches that as a switch grows, meaning that the switching capacity of the switch may be expanded to handle an increase in bandwidth, the size of the switch becomes unwieldy to implement. Cyr teaches an ATM switch 100 comprises an expansion module 200 and receives n inputs, each providing a stream of ATM cells at a predetermined maximum rate. Each input is interconnected internally to the expansion module 200 via a respective one

of the routing processors. A routing processor 55, responsive to receipt of a cell via an associated data path, prepends to the cell header routing information identifying a particular one of the packet switch modules 300 that will forward the cell to its intended destination. The resulting cell is then supplied to the concentrator units contained in expansion module 200. The outputs of the concentrators are then supplied to respective packet switch modules 300 based on the prepended routing information. See column 2, lines 19-38.

Expansion module 200 includes a plurality of conventional cell multiplexer/cell slicing units 60, a plurality of the expand/concentrator unit 70 in a plurality of conventional segment combiner circuits 80. Each multiplexer/cell slicer units serves n/k inputs such that a stream of data cells may be received by each input. When a cell is received in one of the inputs, a multiplexer/cell slicer unit strips off the aforementioned prepending routing information and supplies the information to each expand/concentrator unit via an associated one of the multi-lead buses 10. Thus, each expand/concentrator unit 70 receives the same routing information about a single cell. See column 2, lines 43-62. Consequently, Cyr does not teach the limitation of "a striper sending different portions of the packet as stripes to each fabric", only the same routing information about a single cell to each expand so as concentrator unit 70.

Each multiplexer/slice cell slicer units 60 also multiplexes the cells of the receives via its associated imports until a single stream of cells having a bandwidth of Rn/K. where R is the bandwidth of each input line, n is the total number of inputs 50 and k is the number of packet switch modules 300. Cell multiplier/cell slicer unit 60 then segments each multiplexer cell into j segments and supplies the segments to expand/concentrator circuit 70. Specifically, when a segment arrives at the input of an expand/concentrator unit 70, the segment fans out to k concentrator logic units. At such fan out of a segment, internal to the expand/concentrator unit 70. Each concentrator logic unit than either accepts and stores or discards the segment that it receives at its input based on the associated routing information received via a lead of a respective one of the control bosses 10. See column 20, lines 10-30.

Cyr also does not teach or suggest the limitation that "sends a parity stripe to perform error detection and correction to the parity fabric," as found in Claim 1. In fact, Cyr is totally silent regarding this limitation. Cyr could care less about such a limitation. Again, what Cyr is concerned about is to be able to grow the switch in an efficient manner.

The Examiner is combining Sindhu and Cyr to arrive at Claim 1 of applicants. However, it is respectfully submitted there must be some teaching or suggestion within the references themselves to combine the teachings the Examiner is relying upon to arrive at applicants' invention of Claim 1.

It is respectfully submitted the Examiner is using hindsight to arrive at applicants' claimed invention. Hindsight is not patent law. The Examiner is using the limitations of Claim 1 as a road map to find the various limitations in the disparate references, and having supposedly found these different limitations and the different references, concludes that applicants' claimed invention is arrived at. That is the only reason why an architecture with a single switch (Sindhu) would even be attempted to be combined with an architecture that splits cells and sends the same information about each cell to each expand/concentrator.

Furthermore, the Examiner cannot take the teachings from these references out of the context in which they are found. Applicants do not suggest that they discovered the use of a plurality of switches. Applicants do take the position that their use of a plurality of fabrics in conjunction with the striper and the transfer mechanism and the other limitations of Claim 1 are novel and unique. By following the law, taking the teachings in the context in which they are found, the teachings of the references of the applied art cannot be combined. The context of Cyr is in regard to an expansion module that sends a cell it receives only to the corresponding expand/concentrator unit. In contrast, Sindhu teaches the data from the input ports are all directed to input switch 100 which then sends the data on to the memory 104. These contexts are very distinct and cannot be combined.

The question must also be raised why would one skilled in the art attempt to modify the architecture taught by Sindhu with the architecture taught by Cyr since there is absolutely no need, teaching or suggestion of the input switch 100 being changed into a plurality of switches. This is in direct conflict with the very teachings of Sindhu which requires all input ports to be connected to the single input switch 100. It will require significant research and development to take the teachings of Cyr in the context in which they are found and apply them to the teachings of Sindhu to make an operational system. This only further supports applicants' position that Claim 1 is not obvious from the applied art of record. Accordingly, Claim 1 is patentable over the applied art of record.

Claims 3-8 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable.

Claim 14 is patentable for the reasons Claim 1 is patentable.

Claims 16 and 20 are dependent to parent Claim 14 and are patentable for the reasons Claim 14 is patentable.

The Examiner has rejected Claims 9 and 21 as being unpatentable over Sindhu in view of Cyr and Diaz. Applicants respectfully traverse this rejection. Claims 9 and 21 are

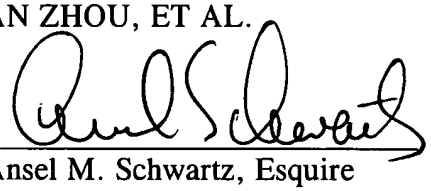
dependent to parent Claims 1 and 14, respectively, and are patentable for the reasons Claims 1 and 14 are patentable. Diaz adds nothing in relevant part to the teachings of Cyr and Sindhu to arrive at applicants' claimed invention.

The Examiner has indicated Claims 25 and 26 are allowed.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1, 3-14 and 16-26, now in this application be allowed.

Respectfully submitted,

FAN ZHOU, ET AL.

By 

Ansel M. Schwartz, Esquire
Reg. No. 30,587
One Sterling Plaza
201 N. Craig Street
Suite 304
Pittsburgh, PA 15213
(412) 621-9222

Attorney for Applicants